해외석학 초청세미나

Low-Latency Preemptive Transaction Scheduling with Userspace Interrupts

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Abstract :

Everything takes time in a database engine: I/O, memory stall, synchronization and admission control all add additional delays in addition to running transaction logic. While most work has focused on hiding latencies caused by stalls and synchronization, in mixed workloads the impact of admission control becomes more pronounced. This talk will revisit the idea of preemptive scheduling for database systems - a technique that was discouraged - and elaborate how it is now desirable with new userspace interrupts and modern concurrency control protocols. We will also emphasize on the practical considerations and workarounds necessary for user interrupts to work with existing database system designs.

Biography :

Tianzheng Wang is an associate professor in the School of Computing Science at Simon Fraser University in Metro Vancouver, Canada. His research centres around the making of database systems in the context of modern hardware, new programming primitives, and new applications. His work also often extends to related areas such as operating systems, parallel programming and distributed systems. Tianzheng Wang received his Ph.D. (2017) and M.Sc. (2014) degrees in Computer Science from the University of Toronto, and B.Sc. (2012) in Computing degree (First Class Honours) from Hong Kong Polytechnic University. His work has been assimilated by cloud vendors and startups, and recognized by awards such as ACM SIGMOD Best Paper Award (2025), ACM SIGMOD Research Highlight Awards (2021 and 2023), and 2019 IEEE TCSC Award for Excellence in Scalable Computing (Early Career Researchers).

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